REMARKS

Claim 45 has been amended. Claims 1-123 remain pending in the present application, and are presented to the Examiner for re-examination in light of the amendments and remarks made herein.

The Examiner rejected claims 1-23, 45-57, and 59-100 under 35 U.S.C. §103(a) as being unpatentable over Dai (U.S. Patent No. 5,877,076) in view of Liou et al. (U.S. Patent No. 5,847,460). Applicant respectfully traverses this rejection.

In the rejection, the Examiner alleges that Dai discloses forming a dielectric layer (120), forming a SiN layer (130) over the dielectric layer (120), and forming a photoresist layer (150) above the SiN layer (130). The Examiner further contends that Dai teaches to form an opening (151) in the photoresist layer (150), etching into the SiN layer (130), removing the photoresist layer (150), and perfoming a second etch pattern in the dielectric layer (120).

The Examiner states that Dai does not disclose that the etching steps are anisotropic etching steps. The Examiner then relies on Liou for teaching the use of anisotropic etch procedures in a semiconductor manufacturing process, and alleges that it would have been obvious to modify the process of Dai by specifically utilizing anisotropic etching because of the advantages anisotropic etching provides over other etching methods.

Applicant respectfully submits, however, that even if it would be considered obvious to combine the teaching of Liou to perform anisotropic etching in the process of Dai as alleged by the Examiner, which Applicant maintains is not necessarily the case, that the limitations of independent claims 1, 45, and 59 of the present invention would still not be met by the alleged

combination as proposed by the Examiner. Applicant respectfully submits in Dai that the portion of the SiN layer 130 (which the Examiner appears to be reading on Applicant's claimed "cap layer") in the etched region of Figure 3g is completely removed. In accordance with the present invention as defined by independent claims 1, 45, and 59, however, a portion of the cap layer is left in the etched region after the first anisotropic etch is performed. Applicant discloses on page 10, lines 14-22 of the specification that the portion of the cap layer in the etched region that remains after the anisotropic etching process protects the process layer residing below from any contamination or damage resulting from the removal of the photoresist layer that resides above the cap layer. In Dai, however, (even when incorporating the anisotropic etch procedure of Liou as proposed by the Examiner) removes the entire portion of the etched region of the SiN layer 130 down to the dielectric layer 120 that resides below the SiN layer 130. That is, the etching procedure completely exposes the dielectric layer 120. In the present invention, however, as defined by independent claims 1, 45, and 59, a portion of the cap layer in the etched region is left to protect any contamination or damage that may result from the subsequent removal of the photoresist layer that resides above the cap layer. Independent claim 1 of the present invention specifically recites "performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, *leaving a portion of the cap layer in the etched region*" (emphasis added). Claim 45 specifically recties "performing a first anisotropic etch into a region of the second process layer underlying the opening in the mask, *leaving a portion of the second process layer in the etched region*" (emphasis added). And, claim 59 specifically recites "performing a first anisotropic etching process into a region of the cap layer underlying the first opening in the first photoresist layer to form an etched region in the cap layer, *leaving a portion of the cap layer in the etched region*"

(emphasis added). Accordingly, because the alleged combination of Dai and Liou as proposed by the Examiner fails to teach leaving a portion of the cap or second process layer in the etched region as a result of the first etch, Applicant respectfully submits that the alleged Dai/Liou combination does not make obvious independent claims 1, 45, and 59 of the present invention. Accordingly, Applicants respectfully submit that independent claims 1, 45, and 59 of the present invention, and all claims dependent thereon, are allowable over the alleged combination of Dai/Liou for at least this reason.

With regard to claim 78 of the present invention, the Examiner acknowledges that Dai fails to teach the deposition of a second cap layer. The Examiner then states that it would have been obvious to modify Dai by utilizing more than one SiN layer with the expectation of achieving the highest possible degree of selectivity during etching. Applicant respectfully submits, however, Dai does not teach to include more than one SiN layer. Moreover, the Examiner has failed to provide a reference providing evidence that it is known in the art to form more than one cap layer as defined by claim 78 of the present invention. Applicant respectfully submits that the only motivation to form more than one cap layer is by the benefit of Applicant's own disclosure. It is well-settled that a reference must provide some motivation or reason for one skilled in the art, working without the benefit of hindsight reconstruction using the Applicants' specification, to make the necessary changes in the disclosed device or method. The mere fact that a reference may be modified in the direction of the claimed invention does not make the modification obvious unless the reference expressly or impliedly teaches or suggests the desirability of the modification. *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984); *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. App. 1985); *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. App. 1984). Indeed, the Federal Circuit stated:

> ... To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction--an illogical and inappropriate process by which to determine patentability. *W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). The invention must be viewed not after the blueprint has been drawn by the inventor, but as it would have been perceived in the state of the art that existed at the time the invention was made. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985).
>
> *Sensonics Inc. v. Aerosonic Corp.*, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996).

Accordingly, because the Examiner has failed to provide evidence that it is known to form more than one cap layer, and because the Examiner has relied on impermissible hindsight to reconstruct Dai to include more than one cap layer, Applicant respectfully submits that the rejection of claim 78, and all claims dependent thereon, is improper and should be withdrawn.

The Examiner rejected claims 22-44 and 58 under 35 U.S.C. §103(a) as being unpatentable over Dai (U.S. Patent No. 5,877,076) in view of Liou et al. (U.S. Patent No. 5,847,460), and further in view of Chiang et al. (U.S. Patent No. 5,817,572). Applicant respectfully traverses this rejection.

The Examiner contends that the combination of Dai/Liou (discussed above) discloses the formation of an opening in the dielectric material and forming a conductive material in the opening. The Examiner acknowledges that the Dai/Liou combination fails to disclose the formation of a barrier layer. The Examiner then relies on Chiang for teaching a semiconductor manufacturing process that includes the step of forming an opening, filling the opening with a barrier layer that includes titanium nitride and then with a conductive layer, and further discloses that the barrier layer functions to separate the dielectric material from the conductive material, thus acting as a "diffusion barrier." The Examiner then alleges that it would have been obvious to modify the Dai/Liou combination by utilizing a barrier layer above the sidewall of the opening

in the dielectric layer, as allegedly taught by Chiang, because it results in an improved separation between the dielectric and conductive materials. Applicant, however, respectfully traverses this rejection.

Applicant respectfully submits that even if Chiang did teach to form an opening, fill the opening with a barrier layer and then a conductive layer, and furthermore, assuming that it would be obvious to combine the teachings of Dai and Liou with Chiang, Applicant submits that not all of the limitations of independent claim 24 have been met. Applicant respectfully submits that the combination of Dai/Liou/Chiang as proposed by the Examiner still fails to teach to leave a portion of the cap layer in the etched region after performing the first anisotropic etch (as discussed in detail above). Independent claim 24 specifically recites "performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, *leaving a portion of the cap layer in the etched region*" (emphasis added). Accordingly, because the alleged combination of Dai, Liou, and Chiang as proposed by the Examiner fails to teach leaving a portion of the cap layer in the etched region as a result of the first etch, Applicant respectfully submits that the alleged Dai/Liou/Chiang combination does not make obvious independent claim 24 of the present invention. Accordingly, Applicants respectfully submit that independent claim 24 of the present invention, and all claims dependent thereon, are allowable over the alleged combination of Dai/Liou/Chiang for at least this reason.

The Examiner rejected claims 101-123 under 35 U.S.C. §103(a) as being unpatentable over Dai (U.S. Patent No. 5,877,076) in view of Liou et al. (U.S. Patent No. 5,847,460), and further in view of Nguyen (U.S. Patent No. 5,821,169). Applicant respectfully traverses this rejection.

The Examiner contends that the combination of Dai/Liou (discussed above) fails to disclose the deposition of a hard mask layer between dielectric layers. The Examiner then relies on Nguyen for teaching a semiconductor manufacturing method wherein a hard mask is deposited over a dielectric layer, and wherein the hard mask has at least one opening to reveal an integrated circuit area. The Examiner further contends that Nguyen discloses that hard mask layers have been used to alleviate the effects of faceting in the transfer of a photoresist pattern to an inter-level dielectric, and that a hard mask profile can further improve the etch and via wall profiles etched into an inter-level dielectric. The Examiner then alleges that it would have been obvious to modify the combination of Dai and Liou by utilizing a hard mask layer having an opening, as is allegedly taught by Nguyen, because the use of hard mask layers have many advantages, including an advanced finished product, which is extremely desirable during semiconductor manufacturing. Applicant, however, respectfully traverses this rejection.

Applicant respectfully submits that even if Nguyen did teach to deposit a hard mask over a dielectric layer, and furthermore, assuming that it would be obvious to combine the teachings of Dai and Liou with Nguyen, Applicant submits that not all of the limitations of independent claim 101 have been met. Applicant respectfully submits that the combination of Dai/Liou/Nguyen as proposed by the Examiner still fails to teach to leave a portion of the cap layer in the etched region after performing the first anisotropic etch (as discussed in detail above). Independent claim 101 specifically recites "performing a first anisotropic etching process into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, leaving *a portion of the cap layer in the etched region*" (emphasis added). Accordingly, because the alleged combination of Dai, Liou, and Nguyen as proposed by the Examiner fails to teach leaving a portion of the cap layer in the etched region as a result of

the first etch, Applicant respectfully submits that the alleged Dai/Liou/Nguyen combination does not make obvious independent claim 101 of the present invention. Accordingly, Applicants respectfully submit that independent claim 101 of the present invention, and all claims dependent thereon, are allowable over the alleged combination of Dai/Liou/Nguyen for at least this reason.

Applicants respectfully submit that the rejections set forth in the present application are improper and should be withdrawn because the cited references fail to teach or suggest all of the limitations of the claims as discussed in detail above. Accordingly, in view of the remarks presented herein, a Notice of Allowance is respectfully solicited.

It is believed that no additional fees are due in connection with filing this paper; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.060900.

The Examiner is invited to contact the undersigned at (713) 934-4058 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

George J. Oehling
Reg. No. 40,471

WILLIAMS, MORGAN & AMERSON
7676 Hillmont, Suite 250
Houston, Texas 77040
(713) 934-7000

Date: 9/30/02

APPENDIX A

45. (Amended) A method for forming a conductive interconnect in a semiconductor device, comprising:

forming a first process layer above a semiconductor substrate;

forming a second process layer above the first process layer;

forming a mask above the second process layer, the mask having an opening therein;

performing a first anisotropic etch into a region of the second process layer underlying the opening in the mask, leaving a portion of the second process layer in the etched region;

removing the mask from above the second process layer;

performing a second anisotropic etch to form an opening in the first process layer; and

forming a conductive material in the opening in the first process layer.